



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/650,604	08/30/2000	Thomas J. Krutsick	5	9105

7590 04/17/2003

Lucent Technologies Inc
Docket Administrator Rm 3C 512
PO Box 636
600 Mountain Avenue
Murray Hill, NJ 07974-0636

[REDACTED] EXAMINER

SEFER, AHMED N

[REDACTED] ART UNIT [REDACTED] PAPER NUMBER

2826

DATE MAILED: 04/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/650,604	KRUTSICK, THOMAS J.
	Examiner	Art Unit
	A. Sefer	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
 THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 13 February 2003.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 28-30 and 32-39 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 28-30 and 32-39 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ .
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .	6) <input type="checkbox"/> Other: _____

DETAILED ACTION***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/3/20003 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 28-30 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo US Patent No. 4,609,935 in view of Davis et al. US Patent No. 5,200,733.

Kondo discloses (see figs. 6-10 and col. 6, lines 46-49) an integrated circuit having a field-plated resistor, the field-plated resistor comprising a resistor body 35 formed in a semiconductor substrate, the resistor body having first and second contact regions, a first insulating layer 33 over the resistor body, the first insulating layer having a top surface and a bottom surface, with the bottom surface in contact with the resistor body, and approximately coextensive therewith, a contact window in the first insulating layer (not shown) and extending from the top surface of the first insulating layer through the first insulating layer through the first

insulating layer to the resistor body, a field plate 39 comprising polysilicon (as in claim 29) on the first insulating layer and approximately coextensive therewith and with the resistor body, the field plate having a top surface and a bottom surface, a second insulating layer 42, with a first portion of the second insulating covering the field plate, an electrical contact to the top surface of the field plate, an electrical contact to the second contact region of the resistor, and a plurality metal conductors 44 formed on the first portion of the second insulating layer, but omits a portion of the bottom surface of the field plate extending through the contact window

Davis et al disclose (figs. 7-12 and col. 4, lines 39-45) a field plate 18/18' with a portion of the bottom surface extending through a contact window in an insulating layer 14 and into contact with a contact region 44 of a resistor 12.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching Davis et al with Kondo's device, since that would increase the surface area of the resistor region as taught by Davis et al.

As to claim 30, Kondo discloses first and second insulating oxide layers.

As to claim 32, Davis et al. disclose insulative spacer 40 around a field plate.

As to claims 33 and 34, Kondo discloses a barrier layer 41.

4. Claims 35-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo US Patent No. 4,609,935 in view of Davis et al. US Patent No. 5,200,733.

Kondo discloses (see figs. 6-10 and col. 6, lines 46-49) an integrated circuit having a field-plated resistor, the field-plated resistor comprising a resistor body 35 formed in a semiconductor substrate, the resistor body having first and second contact regions, a first insulating layer 33 over the resistor body, the first insulating layer having a top surface and a

bottom surface, with the bottom surface in contact with the resistor body, and approximately coextensive therewith, a contact window in the first insulating layer (not shown) and extending from the top surface of the first insulating layer through the first insulating layer through the first insulating layer to the resistor body, a field plate 39 comprising polysilicon (as in claim 29) on the first insulating layer and approximately coextensive therewith and with the resistor body, the field plate having a top surface and a bottom surface, a second insulating layer 42, with a first portion of the second insulating covering the field plate, a metal layer comprising an electrical contact to the top surface of the field plate, an electrical contact to the second contact region of the resistor, and a plurality metal conductors 44 formed on the first portion of the second insulating layer, but omits a portion of the bottom surface of the field plate extending through the contact window.

Davis et al disclose (figs. 7-12 and col. 4, lines 39-45) a field plate 18/18' with a portion of the bottom surface extending through a contact window in an insulating layer 14 and into contact with a contact region 44 of a resistor 12.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching Davis et al with Kondo's device, since that would increase the surface area of the resistor region as taught by Davis et al.

As to the method claims 36-39, the device of claims 28 and 35 would necessarily have to be used in order to achieve their intended function. Claims 36-39 fail to further limit the device of claims 28 and 35 other than simply recite the utilization of the components.

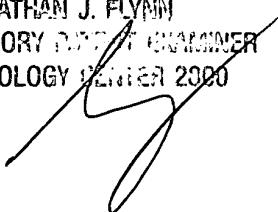
Art Unit: 2826

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601.

ANS
April 9, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2000

A handwritten signature in black ink, appearing to read "NATHAN J. FLYNN". It is written in a cursive style with a large, sweeping flourish at the end.